CLAIMS

What is Claimed is:

1. An integrated circuit (IC) comprising:

a primary substrate having a top surface, a bottom surface, and a plurality of side surfaces;

a plurality of contacts on the top surface of the primary substrate connectable to pins of a packaging element; and,

a capacitive coating on at least the bottom surface of the primary substrate to make contact with a lead frame intended to secure the primary substrate to the packaging element.

2. The IC of claim 1, wherein the capacitive coating has a capacitance that is lower than an internal capacitance of the IC.

3. The IC of claim 1, wherein the capacitive coating extends from the bottom surface to the plurality of side surfaces of the primary substrate.

4. The IC of claim 1, wherein the capacitive coating is a capacitive dielectric.

5. The IC of claim 4, wherein the capacitive dielectric has a low k value.

6. The IC of claim 1, wherein the capacitive coating has a thickness of between 0.01 millimeters and 1.0 millimeters.

7. The IC of claim 1, wherein the capacitive coating has a thickness of substantially 0.1 millimeters.

8. An electronic device comprising:

a packaging element having a number of pins to externally connect the electronic device;

an integrated circuit (IC) having a top surface, a bottom surface, and a plurality of side surfaces;

a plurality of contacts on the top surface of the IC and connected to the pins of the packaging element;

a capacitive coating on at least the bottom surface of the IC; and,

a lead frame to secure the IC to the packaging element, the capacitive coating sandwiched between the IC and the lead frame.

9. The electronic device of claim 8, wherein the capacitive coating has a capacitance that is lower than an internal capacitance of the IC.

10. The electronic device of claim 8, wherein the capacitive coating extends from the bottom surface to the plurality of side surfaces of the IC.

11. The electronic device of claim 8, wherein the capacitive coating is a capacitive dielectric.

12. The electronic device of claim 11, wherein the capacitive dielectric has a low k value.

13. The electronic device of claim 11, wherein the capacitive coating has a thickness of between 0.01 millimeters and 1.0 millimeters.

14. The electronic device of claim 11, wherein the capacitive coating has a thickness of substantially 0.1 millimeters.

15. A method comprising:

coating at least a bottom surface of an integrated circuit (IC) with a capacitive dielectric having a low k value;

connecting a plurality of contacts on a top surface of the IC to corresponding pins of a packaging element; and,

securing the bottom surface of the IC, with the capacitive dielectric, to a lead frame;

securing the lead frame to the packaging element, such that the capacitive dielectric is sandwiched between the IC and the lead frame.

16. The method of claim 15, further comprising performing electrostatic discharge (ESD) testing on the IC.

17. The method of claim 16, wherein performing the ESD testing on the IC comprises performing charged device model (CDM) testing on the IC.

18. The method of claim 15, wherein coating at least the bottom surface of the IC with the capacitive dielectric comprises coating the bottom surface, and at least substantially one or more side surfaces, of the IC with the capacitive dielectric.

19. The method of claim 15, wherein coating at least the bottom surface of the IC with the capacitive dielectric comprises coating at least the bottom surface of the IC with the capacitive dielectric such that the dielectric has a thickness of between 0.1 millimeters and 1.0 millimeters.

20. The method of claim 15, wherein coating at least the bottom surface of the IC with the capacitive dielectric comprises coating at least the bottom surface of the IC with the capacitive dielectric such that the dielectric has a thickness of substantially 0.1 millimeters.